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S13	0	"nickel on cobalt silicide"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/07 09:06
S14	0	"nickel deposited on cobalt silicide"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/07 09:06
S15	2539	(nickel or iron) and cobalt and gate adj electrode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/07 09:07

Formation and Properties of ternary silicide $(Co_xNi_{1-x})Si_2$ thin films

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Abstract

A ternary silicide $(Co_xNi_{1-x})Si_2$ formed by Ni and Co thin films or Ni, Co and Ti thin films deposited on Si(100) substrate is studied. The results show that a high conductive silicide $(Co_xNi_{1-x})Si_2$ can be formed by solid phase reaction of either Ni/Co/Si or Co/Ni/Si structure. The resistivity of the silicide films is in range of (15-20) $\mu\Omega$•cm. The formation temperature of $(Co_xNi_{1-x})Si_2$ is rather low compared with the disilicides of Co and Ni. XRD data show that $(Co_xNi_{1-x})Si_2$ has a CaF_2 structure and its lattice constant is between that of $CoSi_2$ and $NiSi_2$. $(Co_xNi_{1-x})Si_2$ can also be formed by rapid thermal annealing of a Co/Ni/Ti/Si multilayer structure. A quite low χ_{min} value is shown by RBS/channeling investigation. The film has a better epitaxy quality as compared with that without a Ti interlayer. It is more uniform and has a good thermal stability and low resistivity. The experiments with two step annealing and chemical selective etching demonstrate the self-aligned silicided contact and gate-level interconnection structure can be formed on Si wafer..

Introduction

Contact and interconnect technology is one of the key issues in submicron and deep submicron integrated circuits(IC). Metal silicides can be employed to reduce both the resistance of source/drain region and gate level interconnection of CMOS IC. Self-aligned silicide (Salicide) technology in which silicide is formed simultaneously on source/drain and gate regions of MOS devices, has been widely used in very large and ultra large integrated circuits(VLSI/ULSI) fabrication. $TiSi_2$ has become the most popular silicide for this application, mainly because of its low resistivity.[1] It has been found, however, that the sheet resistance(Rs) of titanium silicides may increase significantly as the line width decreases.[2] An alternative for $TiSi_2$ in deep submicron salicide technology has not found yet. Both $CoSi_2$ and NiSi are attractive candidate for this purpose.[3-4] For $CoSi_2$, the gate sheet resistance may increase at very narrow width due to the thinning of CoSi2 films at the edge of polySi line. At the same time, the formation of $CoSi_2$ consumes more Si than $TiSi_2$, which is unfavorable for ultra-shallow junction. NiSi has the similar low resistivity as $TiSi_2$ and $CoSi_2$, but it requires a low post-silicide processing temperature. When the annealing temperature is above 750°C, NiSi will transform into $NiSi_2$, which has a undesirable higher resistivity.

$(Co_xNi_{1-x})Si_2$ can be formed by solid reaction of Ni and Co bilayers deposited on Si(100) and was considered as a solid solution of $CoSi_2$ and $NiSi_2$.[5,6] Both $CoSi_2$ and $NiSi_2$ have CaF_2 structure and their lattice constants at room temperature are 5.364Å and 5.406Å respectively. which are very close to that of silicon. They can be epitaxially grown on silicon substrate. In this study (Co-Ni)Si_2 of tens of nano-meters is formed by rapid thermal annealing(RTA) structure Ni/Co/Si or Co/Ni/Si. Their electrical and physics properties are studied.

Experimental procedures

In the experiments n-type Si(100) wafers with resistivity of 5-8 Ω•cm were used as the substrates. After standard RCA cleaning. the wafers were dipped in diluted HF for 30 seconds to remove the residual oxide on the surface. Then the wafers were loaded into the Oxford ion beam sputtering system. The base pressure is lower than 7×10^{-7} Torr and the metal layers were deposited at a pressure of 5×10^{-5} Torr All the samples were annealed ex situ in N_2 ambient using a RTA system. The sheet resistance was measured with a four-point probe at room temperature. Solutions of $H_2SO_4+H_2O_2$(1:1) or $HCL+H_2O_2$(1:1) are applied to selectively etch the unreacted metal. Selected samples were characterized by Auger electron spectroscopy(AES) to determine the Co:Ni:Si ratio and the compositional uniformity along the thickness of the film. The crystalline phase and quality of $(Co_xNi_{1-x})Si_2$ were investigated by X-ray diffraction(XRD) and Rutherford backscattering spectrometry(RBS). The RBS analysis was carried out using 2Mev He^+ ions at both random and aligned (channeling) incidence. The patterned samples after selective etching is investigated by scanning electron microscope(SEM).

Results and discussions

1. lattice structure

Ternary silicide $(Co_xNi_{1-x})Si_2$ can be formed by annealing structure Co/Ni/Si or Ni/Co/Si in N_2 ambient. This is demonstrated by XRD data. Fig.1 shows the X-ray diffraction pattern of structure Ni(10nm)/Co(10nm)/Si after heat treatment at 900°C for 1 minute in N_2 ambient.

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There are two reflections with high intensity near the

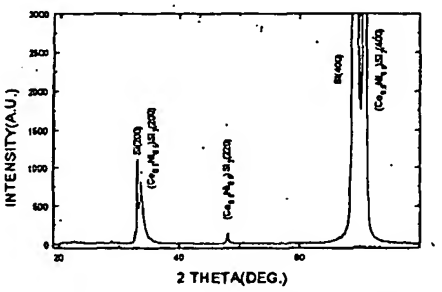

Fig.1. XRD spectrum of sample Ni(10nm)/Co(10nm)/Si(100) annealed at 900°C for 1 minute in N_2.

reflections of Si(200) and Si(400) respectively, which are very similar to that of epitaxial $CoSi_2$ or $NiSi_2$. In fact, a ternary silicide $(Co_xNi_{1-x})Si_2$, in this case $(Co_{0.5}Ni_{0.5})Si_2$, is formed. $(Co_xNi_{1-x})Si_2$ has the same crystal structure of CaF_2 as $NiSi_2$ or $CoSi_2$. The XRD spectrum indicates this ternary silicide film is preferentially and epitaxially grown. The lattice constant is 5.324Å, which is between that of $NiSi_2$ and $CoSi_2$ films formed by same process and with similar thickness. A strain is formed during the reaction and this strain cause the atomic planes to shrink. So atomic plane distance measured by XRD is smaller than the standard values. For another sample of structure Co(10nm)/Ni(5nm)/Si heat treated at 900°C for 1 minute, XRD shows a smaller lattice constant of 5.319Å. As the percentage of Ni increasing, the lattice of $(Co_xNi_{1-x})Si_2$ becomes bigger and larger to that of $NiSi_2$.

2. formation temperature by RTA

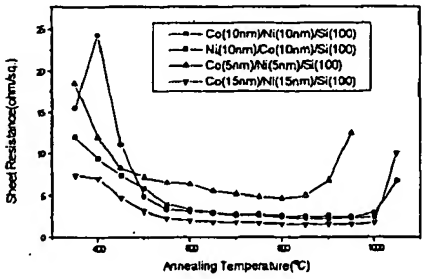

Fig.2. Sheet resistance variation of Ni/Co/Si and Co/Ni/Si with annealing temperature.

From XRD spectrum, an annealing temperature of 900°C is high enough to form $(Co_xNi_{1-x})Si_2$. $(Co_xNi_{1-x})Si_2$ is a low resistivity phase.[5] Fig.2 show the sheet resistance variation of structure Ni/Co/Si and Co/Ni/Si with annealing temperature. After 550°C, 1 minute heat treatment, the sheet resistance of all samples decrease to a low value. This indicates the low resistivity phase have been formed. The formation temperature of $(Co_xNi_{1-x})Si_2$ is around 550°C. It is relatively low as compared to $CoSi_2$, whose forming temperature is 700°C by RTA. For samples with structure Ni/Co/Si, after 400°C, 1 minute heat treatment, its sheet resistance rise higher as compared with structure Co/Ni/Si. During solid reaction, Ni diffuse to Si substrate. A high resistivity alloy layer of Ni and Co is thus formed. When the annealing temperature rise higher, two separate phase of NiSi and CoSi are formed.[5] Figh.3 is AES depth profile of

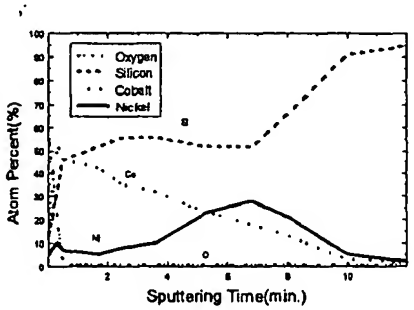

Fig.3. AES depth profile of structure Co(20nm)/Ni(20nm)/Si(100) annealed at 500°C, 2 minutes.

structure Co(20nm)/Ni(20nm)/Si annealed at 500°C, 2 min. Two monosilicide of NiSi and CoSi are formed, with NiSi Closer to Si substrate. The AES depth profile of structure Ni(20nm)/Co(20nm)/Si after 500°C, 2 minutes shows similar result. $(Co_xNi_{1-x})Si_2$ can be formed by annealing structure Co/Ni/Si or Ni/Co/Si. As the treating temperature rise, firstly a high resistivity phase, then two separate monosilicides, and a ternary silicide $(Co_xNi_{1-x})Si_2$ is formed.

3. Titanium interlayer mediated epitaxy(TIME)

$(Co_xNi_{1-x})Si_2$ formed by annealing structure Ni/Co/Si or Co/Ni/Si is preferentially grown on Si(100) and has epitaxial character. But the epitaxial quality is not good. For a sample with structure Ni(20nm)/Co(20nm)/Si annealed at 950°C for 2 minutes, RBS/channeling investigation shows the channeling minimum yield χ_{min} is 86%. From XRD spectrum in fig.1, there are $(Co_xNi_{1-x})Si_2(220)$ reflections.

The TIME method can improve the epitaxy quality of $CoSi_2$ and it's compatible with present salicide technology.[6] In this work, we apply TIME to improve the epitaxy quality of $(Co_xNi_{1-x})Si_2$. Fig.4 shows RBS/channeling spectra of sample prepared by TIME. The sample of Ni(5nm)/Co(10nm)/Ti(3nm)/Si(100) was firstly annealed at 900°C for 1 minute, then selective etched in $HCL+H_2O_2$ and at last annealed at 1050°C for 10 seconds. After first annealing, Ti diffuse to the surface to react with N_2 and form TiN layer. Ni and Co diffuse

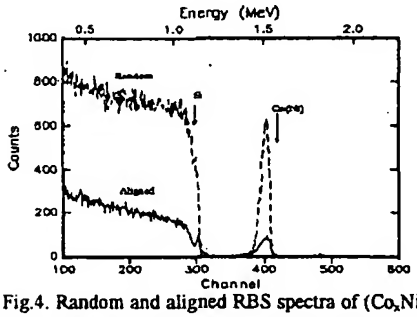

Fig.4. Random and aligned RBS spectra of $(Co_xNi_{1-x})Si_2$ film formed by Co(10nm)/Ni(5nm)/Ti(5nm) /Si(100) reaction.

toward the substrate to form silicide. After the selective etching, TiN layers was etched off. XRD spectrum demonstrate this silicide is $(Co_xNi_{1-x})Si_2$. All the reflections of $(Co_xNi_{1-x})Si_2$ in the XRD spectrum have the same orientation as Si substrate, which indicate a good epitaxial quality. RBS/channeling spectra in fig.4 demonstrate the channeling minimum yield χ_{min} is 14%. The back scattering peaks of Ni and Co can not be distinguished because their atomic weights are so close. This low χ_{min} value show the epitaxial quality is fairly good. So a fairly good epitaxial $(Co_xNi_{1-x})Si_2$ film can be obtained by the TIME method.

4. electrical property

Silicide is used in VLSI for contact and interconnection, so good conductivity and low contact resistivity with Si are required. As shown in fig.2, after RTA treatment, the sheet resistance of $(Co_xNi_{1-x})Si_2$ films drops to a low value. From the sheet resistance we can calculate the resistivity of $(Co_xNi_{1-x})Si_2$. For the samples with (Co:Ni=1:1), the resistivity rises up when the thickness of silicide is below 50nm. This phenomenon may due to oxygen contamination. As shown in the AES depth profile in fig.3, there are oxygen signals near the surface. When the thickness of silicide film decrease, influence of oxygen contamination will be more severe, which may be partly responsible for the increasing of the resistivity.

The resistivity of $(Co_xNi_{1-x})Si_2$ varies with the ratio of

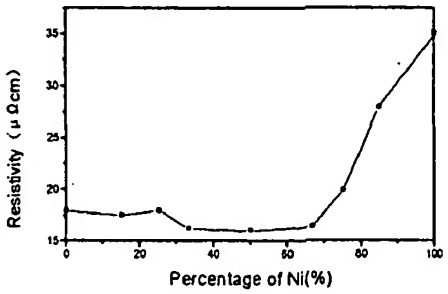

Fig.5. Room temperature resistivity of $(Co_xNi_{1-x})Si_2$ films vary with Ni percentage. $(Co_xNi_{1-x})Si_2$ films were formed by annealing Ni and Co films on Si(100) at 850°C.

Ni/Co, as shown in fig.5. The curve keep low and flat when the percentage of Ni is below 66%. The resistivity increase almost linearly when the percentage of Ni is higher than 66%.

5. salicide process

A silicide must be selective etched in order to be applied in salicide application. Fig.6 show the sheet resistance variation of the samples formed by Co(15nm)/Ni(15nm) /Si(100) after first annealing(curve A), selective etching by $H_2SO_4+H_2O_2$(1:1) at 80°C to remove the unreacted metal. The second high temperature annealing turn the films to low resistivity $(Co_xNi_{1-x})Si_2$ phase. From fig.6, the

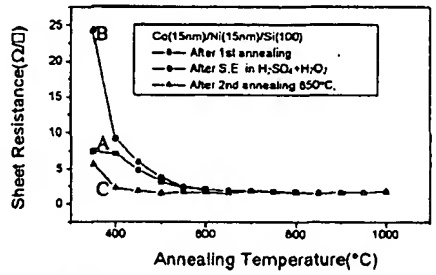

Fig.6. The sheet resistance of Co(10nm)/Ni(5nm)/Si(100) after first step annealing at different temperature, selective etching and second step annealing at 850°C for 2 minutes.

first annealing temperature should be 400°C~550°C for salicide process. Experiments also demonstrate that the unreacted metal films on SiO_2 after first step annealing can be etched off by H_2SO_4+H_2O_2. Fig.7 shows SEM picture of a patterned wafer after 500°C, 120 seconds annealing and selective etching. The wafer was first patterned with 2μm CMOS device structure, then 10nm Co and Ni films were sputtered on it consequently. As shown in fig.7, there is no silicide left on the oxide sidewall. The silicides only grow on the polySi gate and source/drain region. There was not any shortcuts found

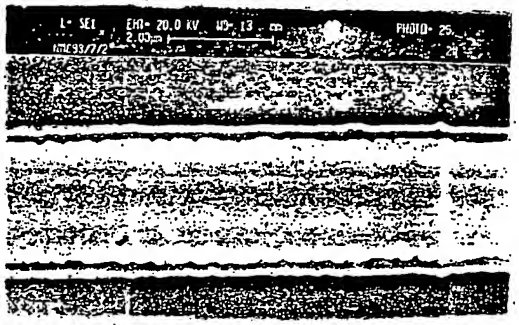

Fig.7. SEM photograph showing no silicide remaining on the SiO_2 sidewalls. The sample was selective etched after annealed at 500°C for 2 minutes.

between gate and source/drain, which cause the failure of the devices. Because the forming temperature of $(Co_xNi_{1-x})Si_2$ is around 550°C, it's hopeful to use one-step annealing at 550°C for salicide process.

6. thermal stability

As the device dimension decrease, the thickness of silicide need to be thinner. The thermal stability of silicide will become worse as its thickness decreases. In this work, the thermal stability of $(Co_xNi_{1-x})Si_2$ thin films is studied and compared with $CoSi_2$ thin film, as shown in fig.8. The thickness of both silicides are about 52.5nm. In this case, $(Co_xNi_{1-x})Si_2$ was formed by annealing Co(10nm)/Ni(5nm)/Si(100). The sheet resistance of both films rise after annealed at high temperature. As the annealing time increase, Rs rises. As shown in fig.8, the sheet resistance of $CoSi_2$ increase more rapidly than that of $(Co_xNi_{1-x})Si_2$, which indicates that $(Co_xNi_{1-x})Si_2$ have a better thermal stability than $CoSi_2$.

Conclusions

Ternary silicide $(Co_xNi_{1-x})Si_2$ has a CaF_2 structure. The XRD measured atomic plane distance is between that of $CoSi_2$ and $NiSi_2$ and increase with the ratio of Ni/Co.

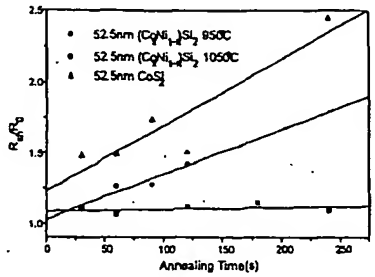

Fig.8. Sheet resistance variation of annealing time at different temperatures. The Rs of CoSi2 and $(Co_xNi_{1-x})Si_2$ with same thickness is compared.

Two-step annealing with a selective etching can form self-aligned $(Co_xNi_{1-x})Si_2$ silicide on patterned Si wafer. $(Co_xNi_{1-x})Si_2$ may be considered as a candidate for contact and interconnection material in VLSI technology.

The addition of an interposed Ti layer can significantly improve the epitaxial quality of $(Co_xNi_{1-x})Si_2$. This process is also compatible with salicide process.

$(Co_xNi_{1-x})Si_2$ thin film has low resistivity as $CoSi_2$, $TiSi_2$ and NiSi, which is in range of 15-20μΩ•cm. Its resistivity varies with x.

The thermal stability of thin $(Co_xNi_{1-x})Si_2$ is better than that of $CoSi_2$ with same thickness.

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